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# Analysis of SRAM and High Speed CAM Based On Reordered Overlapped Search Mechanism

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***Abstract:*** **In this paper, A Novel high speed Analysis of SRAM circuit that employs adiabatic charging of a word line during a read operation was found to provide a large dynamic noise margin (DNM) for reading and CAM memory by using a reordered overlapped search mechanism for high-throughput low-energy. In our circuit implementation in CAM memory cell, each word circuit is independently controlled by a locally generated timing signal rather than a global signal. In SRAM an analysis of the time-wise change in DNM revealed that the read noise margin of this circuit was 1.9 times larger than that of a conventional two-BL circuit. But in asynchronous CAM operates 5.98 times faster than a synchronous CAM with 14.2% smaller energy dissipation.**

***Keywords:*** **Adiabatic, low power, asynchronous circuits, associative memory, NAND-type CAM, RWOS, POP.**

## I. INTRODUCTION

The VLSI circuit designers are need high speed devices to produce good products for Industries. A large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. The memory devices are very helpful to achieve high speed by using low power consumption. In SRAM, reducing the device size by one-half cuts the gate capacitance by one-fourth, which should result in a large reduction in power consumption. CAMs are used for many applications, such as parametric curve extraction, Hough transformation, a human body communication controller**.**

## II. CONCEPT OF SRAM

A conventional SRAM uses two pre-charged BLs for reading. The problem is that the low-voltage node of an FF increases from 0 V. In contrast, a single-BL SRAM uses only one BL for reading. When V1 = 1 andV2 = 0, V2 is not connected to the pre-charged BL; so it remains at a low level. Therefore, a single-BL SRAM has a larger SNM than one with two BLs. The BL is connected to the global bit line (GBL) via the write and read ports [6]. They are activated by the write port switch signal (WPSW) and the read port switch signal (/RPSW). Only the read word line (RWL) goes high during reading, while both the RWL and the write word line (WWL) go high during writing. For reading, the /RPSW is set low. When V1 is low, the GBL increases from the pre-charge voltage to the read-port supply volt- age, VRP; and whenV1 is high, the GBL does not change. In a conventional SRAM, BL and /BL show a small voltage difference.

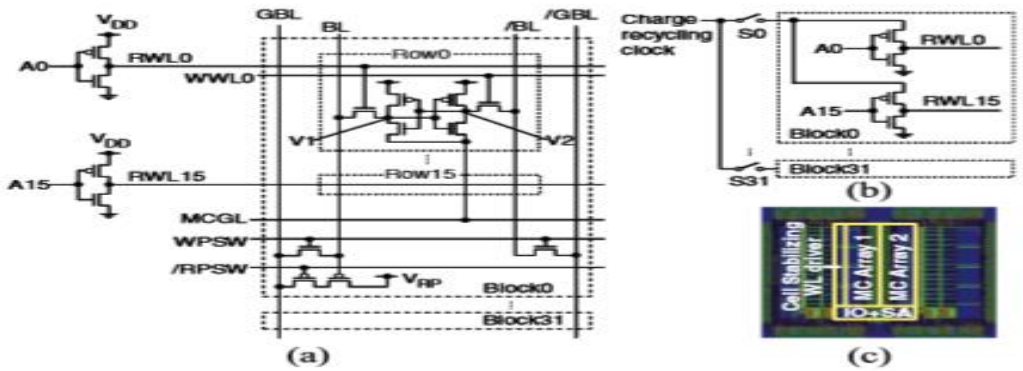


**Fig. 1. (a) SRAM that uses single BL for read operation. (b) WL driver when a charge recycling clock is used. (c) Layout of (a).**

### A. ADIABATIC:

The meaning of the word "adiabatic" needs some explanation. "Adiabatic" is used in thermodynamics and mechanics. In thermodynamics, an adiabatic process is one that produces no heat flow; i.e., there is no Joule heating. For a transistor, that means that it is not turned on when there is a voltage potential. In mechanics, on the other hand, an adiabatic change is a slow deformation of a state in which a certain parameter changes very slowly. In our circuit, that parameter is the WL voltage. So, in the term "adiabatic charging" for the circuit in Fig. 1(a), "adiabatic" has the sense used in mechanics.

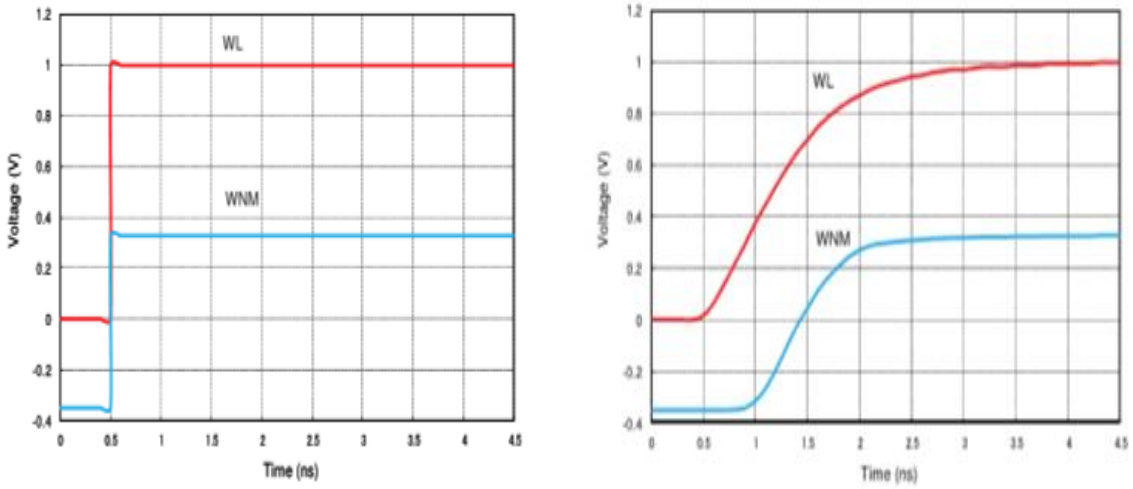


**Fig. 2 WNM versus time for (a). abrupt WL charging. (b) adiabatic WL charging**

Simulations of WNM for abrupt WL charging (Fig. 2a) show that, at t = 0, WNM is negative (−0.35 V). This means that there are two stable states; so a write operation might not be performed correctly. When WL reaches 1 V, WNM becomes positive; so there is only one stable state and a write operation is performed correctly.

Simulations of WNM for adiabatic charging (Fig.2b) show that the initial and final WNM are the same as those for abrupt charging. What is different is the write time: it is about 2 ns for adiabatic charging but <0.1 ns for abrupt charging. Thus, adiabatic operation does not change the WNM, but it does make the write time longer.

## III. CONTENT ADDRESSABLE MEMORY (CAM)

Each input-search bit is compared with its CAM-cell bit and the comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states. CAM cells are classified into two types: NOR type CAM and NAND type CAM. In NAND type pass transistor and ML are connected in series, so it operates in medium speed. In NOR type pass transistor and ML are connected in parallel, so it operates in high speed. A NAND-type word circuit (fig.3b.) reduces the power dissipation of MLs compared to the NOR-type word circuit. Each word block has a match line (ML) that indicates whether search and stored words are the same or different.

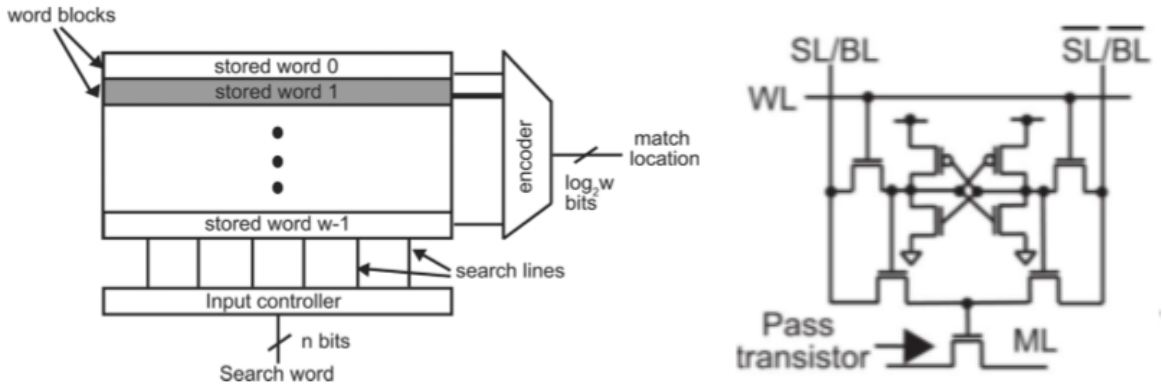


**Fig. 3. (a) Block diagram of content addressable memory (CAM), (b) NAND cell.**

The outputs of the word blocks are fed to an encoder that generates a binary match location corresponding to the ML that is in the match state. In a traditional synchronous CAM, the next search word is assigned after the current search is complete. The operation throughput is restricted by the number of bits of a CAM word because the worst-case delay of a match operation is usually proportional to the number of bits.

## IV. REORDERED OVERLAPPED SEARCH MECHANISM

A reordered overlapped search mechanism that includes two new approaches: a reordered word-overlapped search (RWOS) and phase-over- lapped processing (POP). It contains a CAM block, an input controller, and an output controller. Once input words are re- ordered in the input controller, the input controller sends a signal, which indicates a reordered input word to the output controller. The output controller reorders the output address based on the signal. Once input words are reordered, the output addresses correspond to the input words are reordered, again by indicating which address is replaced.

The RWOS scheme reduces the probability of the slow mode to improve the throughput. In the RWOS scheme, the last bits of a cur- rent search word are compared with the last bits of consecutive search words and an extra search word followed by the current search word. If the consecutive sub-search words are different from the current sub-search word, the CAM operates at the fast mode. Otherwise, one of the sub-search words that is the same as the current sub-search word is replaced by the extra sub-search word. In this case, the extra sub-search word has to be different from the current sub-search word.

In the POP scheme, only the ML of a matched word circuit is charged by a lctrl signal in a pre-charge phase after the matching in the previous evaluate phase. The other word circuits are still in an evaluate phase because their lctrl signals remain high. Using the WOS scheme, consecutive search words are assigned to unused different word circuits that are in an evaluate phase. Hence, input search words can be processed without wasting the pre-charge time.

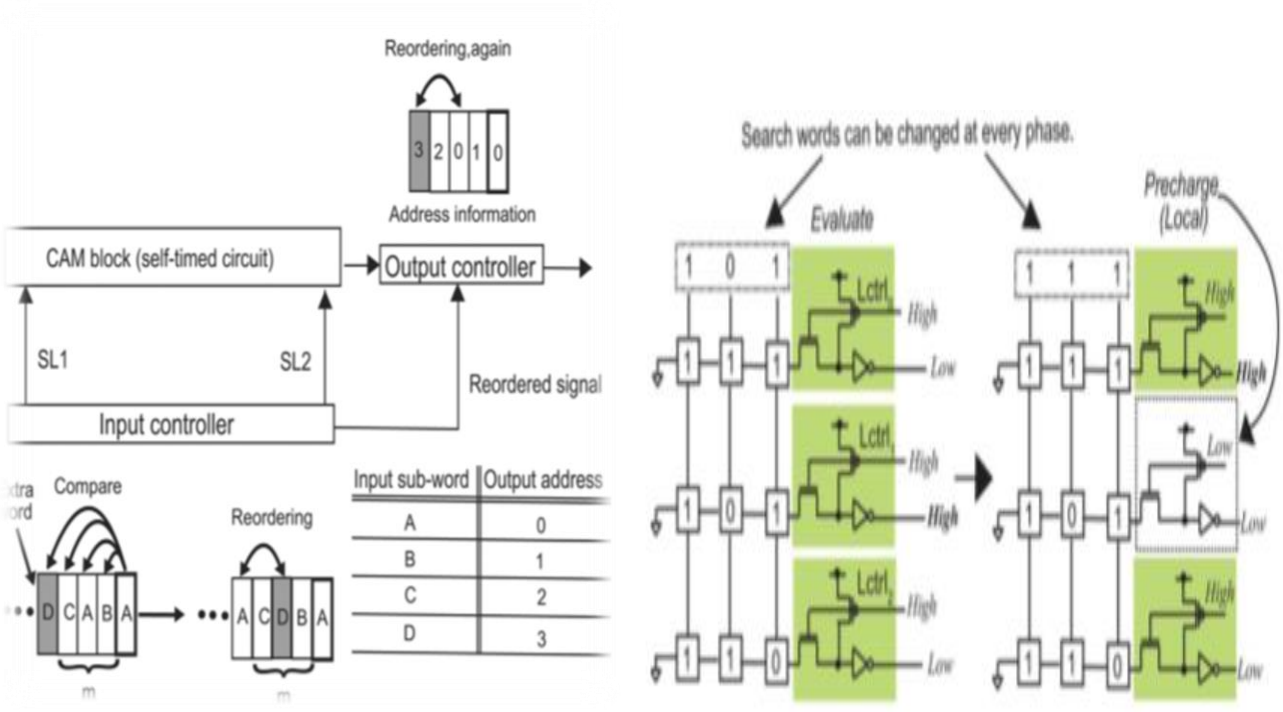


**Fig. 5. High-level structure of the proposed CAM based on the RWOS and the POP schemes.**

**TABLE: I CONVENTIONAL SRAM, ADIABATIC-WLSRAM AND CAM**

| Circuit Type | Conventional SRAM | Adiabatic WL-SRAM | NAND type CAM |
|---|---|---|---|
| Operating cond. | 45 nm, 1 V | 45 nm, 1 V | 32nm, 1V |
| Speed | 300–850 M | 80 MHz | - |
| Number of Transistor | 14 | 14 | 9 |
| Energy Metric(bit/search) | - | - | 0.773 |

## V. CONCLUSION

We Analysed a new SRAM with a small-capacitance BL that employs a shared read port and adiabatic WL charging for reading. Using the RWOS scheme at the scheduling level, the proposed CAM operates at a rate based on the short delay of the last few-bit search rather than the long delay of whole-word search. At the circuit level, the POP scheme hides the delay of a pre-charge phase using local control and hence greatly reduces the cycle time compared with a traditional synchronous CAM.

## REFERENCES

[1] M. Meribout, T. Ogura, and M. Nakanishi, "On using the CAM concept for parametric curve extraction," IEEE Trans. Image Process., vol. 9, no. 12, pp. 2126–2130, Dec. 2000.

[2] M. Nakanishi and T. Ogura, "A real-time CAM-based Hough trans- form algorithm and its performance evaluation," in Proc. 13th Int. Conf. Pattern Recog., Aug. 1996, vol. 2, pp. 516–521.

[3] D. J. Craft, "A fast hardware data compression algorithm and some algorithmic extensions," IBM J. Res. Develop., vol. 42, no. 6, pp. 733–746, Nov. 1998.

[4] S.Choi,S.-J.Song,K.Sohn,H.Kim,J.Kim,N.Cho,J.-H.Woo, J.Yoo, and H.-J. Yoo, "A 24.2-mW dual-mode human body communication controller for body sensor network," in Proc. 32nd Eur. Solid-State Circuits Conf., Sep. 2006, pp. 227–230.

[5] S. Choi, K. Sohn, J. Kim, J. Yoo, and H.-J. Yoo, "A TCAM-based pe- riodic event generator for multi-node management in the body sensor network," in Proc. Asian Solid-State Circuits Conf. 2006, Nov. 2006, pp. 307–310.

[6] P.-F. Lin and J. Kuo, "A 1-V 128-kb four-way set-associative CMOS cache memory using word line-oriented tag-compare (WLOTC) structure with the content-addressable-memory (CAM) 10-transistor tag cell," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 666–675, Apr. 2001.

[7] C.-C. Wang, C.-J. Cheng, T.-F. Chen, and J.-S. Wang, "An adaptively dividable dual-port bit cam for virus-detection processors in mobile devices,"IEEEJ.Solid-StateCircuits,vol.44,no.5,pp.1571–1581,May 2009.

[8] N. Onizawa, W. Gross, and T. Hanyu, "A low-energy variation-tol- erant asynchronous TCAM for network intrusion detection systems," in IEEE 19th Int. Symp. Asynchronous Circuits Syst. (ASYNC), May 2013, pp. 8–15.

[9] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Chou, "Low-power digital systems based on adiabatic-switching principles," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 2, no. 4, pp. 398–407, Dec. 1994.

[10] K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design. New York, USA: Wiley, 2000.

[11] S. Kim and M. C. Papa efthymiou, "True single-phase adiabatic circuitry," IEEE Trans. Very Large Scale Integrated (VLSI) Syst., vol. 9, no. 1, pp. 52–63, Feb. 2001.

[12] .A. Blotti and R. Saletti, "Ultralow-power adiabatic circuit semi-custom design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 11, pp. 1248–1253, Nov. 2004.

[13] S. Nakata, "Adiabatic charging reversible logic using a switched capac- itor regenerator," Inst. Electron. Inf. Commun. Eng. Trans. Electron., vol. E87-C, no. 11, pp. 1837–1846, Nov. 2004.

[14] M. E. Hwang, A. Raychowdhury, and K. Roy "Energy-recovery tech- niques to reduce on-chip power density in molecular nanotechnologies," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 8, pp. 1580–1589, Aug. 2005.

[15] K. Kim, H. Mahmoodi, and K. Roy, "A low-power SRAM using bit- line charge-recycling," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 446–459, Feb. 2008. [16] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra-low- power clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integrated. (VLSI) Syst., vol. 17, no. 1, pp. 33–44, Jan. 2009.